I CLAIM:

1. A process for forming a polycrystalline semiconductor portion on a substrate, the method comprising the steps of:

(a) depositing semiconductor onto the substrate to form a semiconductor layer having an amorphous region;

(b) depositing a metal onto the semiconductor layer to form a structure comprising the substrate, semiconductor layer and a doping metal layer;

(c) annealing the structure at a temperature in the range of about 170°C to about 600°C to convert at least a portion of the amorphous region into polycrystalline semiconductor.

2. The process of claim 1 wherein the semiconductor comprises at least one selected from the group consisting of silicon, germanium, silicon-germanium alloys, germanium-carbon alloys, silicon-carbon alloys, and silicon-nitrogen alloys.

3. The process of claim 2 wherein the semiconductor comprises at least one selected from the group consisting

of silicon, germanium and silicon-germanium alloys.

4. The process of claim 2 wherein the semiconductor comprises silicon.

5. A process for forming a polycrystalline semiconductor layer on a substrate, wherein the substrate comprises a semiconductor layer thereon having an amorphous region, and comprises a metal layer supported on the amorphous semiconductor layer, the method comprising the step of:

(a) annealing the structure at a temperature in the range of about 170°C to about 600°C to convert at least a portion of the amorphous region into polycrystalline semiconductor.

6. The process of claim 5 wherein the semiconductor comprises at least one compound selected from the group consisting of silicon, germanium, silicon-germanium alloys, germanium-carbon alloys, silicon-carbon alloys, and silicon-nitrogen alloys.

7. The process of claim 6 wherein the semiconductor

comprises at least one selected from the group consisting of silicon, germanium and silicon-germanium alloys.

8. The process of claim 6 wherein the semiconductor comprises silicon.

9. Polycrystalline semiconductor comprising greater than about 1×10^{20} aluminum atoms per cm^3 of silicon.

10. In a process for manufacturing a semiconductor device, the improvement of forming a semiconductor junction by a method comprising:

(a) providing a semiconductor substrate;

(b) depositing a layer of amorphous silicon onto said semiconductor substrate to form a structure comprising the semiconductor substrate and the layer of amorphous silicon;

(c) depositing a layer of metal onto said layer of amorphous silicon to form a structure comprising the semiconductor substrate, the layer of amorphous silicon, and the layer of metal; and

(d) without depositing any additional layers onto the metal layer, annealing the structure formed in step (c) at a temperature in the range of about 170°C to about 600°C to convert at least a portion of the amorphous silicon layer into crystalline silicon, wherein the metal promotes the conversion of the at least a portion of the amorphous region into the crystalline silicon to provide a semiconductor junction between said crystalline silicon and said semiconductor substrate.

11. The process of Claim 10, wherein said semiconductor substrate is doped with a dopant of a first

conductivity type and said layer of amorphous silicon is doped with a dopant of a second conductivity type opposite to that of said semiconductor substrate.

12. The process of Claim 10, wherein said temperature in step (d) is less than about 450°C.

13. The process of Claim 12, wherein said temperature in step (d) is in a range of about 200°C to about 300°C.

14. The process of Claim 10, wherein the metal includes a doping metal which serves to promote the conversion of at least a portion of the amorphous silicon layer into the crystalline silicon and to dope the crystalline silicon.

15. The process of Claim 14, wherein the doping metal is aluminum.

16. The process of Claim 14, wherein the doping metal is effective to convert the at least a portion of the amorphous silicon layer from one n-type, intrinsic, or p-type material 6 to another upon crystallization.

17. The process of Claim 16, wherein the doping metal is aluminum.

18. The process of Claim 10, wherein said annealing is conducted for an annealing time in the range of about 1 second to about 24 hours.

19. The process of Claim 18, wherein said annealing is conducted for an annealing time in the range of about 30 seconds to about 1 hour.

20. The process of Claim 19, wherein said annealing is conducted for an annealing time in the range of about 1 minute to about 30 minutes.

21. In a process for manufacturing a semiconductor device, the improvement of forming a p-n junction by a method comprising:

(a) providing a crystalline silicon semiconductor substrate of a first conductivity type;

(b) depositing a layer of amorphous silicon onto said semiconductor substrate to form a structure comprising the semiconductor substrate and the layer of amorphous silicon;

(c) depositing a layer of doping metal onto said layer of amorphous silicon to form a structure comprising the semiconductor substrate, the layer of amorphous silicon, and the layer of doping metal, wherein said doping metal is selected to provide a dopant of a second conductivity type opposite to that of the semiconductor substrate; and

(d) without depositing any additional layers onto the metal layer, annealing the structure formed in step (c) at a temperature in the range of about 170°C to about 600°C to convert at least a portion of the amorphous silicon layer into crystalline silicondoped with the doping metal, wherein the doping metal promotes the conversion of the at least a portion of the amorphous silicon layer into crystalline silicon so as to provide a semiconductor junction between that crystalline silicon and said crystalline silicon substrate.

22. The process of Claim 21, wherein said temperature in step (d) is less than about 450°C.

23. The process of Claim 22, wherein said temperature in step (d) is in a range of about 200°C to about 300°C.

24. The process of Claim 21 , wherein the doping metal is aluminum.

25. The process of Claim 21, wherein the doping metal is effective to convert the at least a portion of the amorphous silicon layer from one of an n-type, intrinsic, or p-type material to another upon crystallization.

26. The process of Claim 25, wherein the doping metal is aluminum.

27. The process of Claim 21, wherein said annealing is conducted for an annealing time in the range of about 1 second to about 24 hours.

28. The process of Claim 27, wherein said annealing is conducted for an annealing time in the range of about 30 seconds to about 1 hour.

29. The process of Claim 28, wherein said annealing is conducted for an annealing time in the range of about 1 minute to about 30 minutes.

30. A process for making a semiconductor junction, comprising:

(a) depositing a semiconductor layer having an amorphous region onto a semiconductor surface;

(b) depositing a layer of metal onto the amorphous region of the semiconductor layer to form a structure comprising the semiconductor surface, the semiconductor layer, and the metal layer; and

(c) without depositing any additional layers onto the metal layer, annealing the structure formed in step (b) at a temperature in the range of about 170°C to about 600°C so as to convert at least a portion of the amorphous region into a crystalline semiconductor having a junction with the semiconductor surface, wherein the metal of a first portion of the metal layer promotes the conversion of the at least a portion of the amorphous region into the crystalline semiconductor.

31. The process of Claim 30, wherein said temperature in step (c) is less than about 450°C.

32. The process of Claim 31, wherein said temperature in step (d) is in a range of about 200°C to about 300°C.

33. The process of Claim 30, wherein the metal includes a doping metal which serves to promote the conversion of at least a portion of the amorphous region into the crystalline semiconductor and to dope the crystalline semiconductor.

34. The process of Claim 33, wherein the doping metal is aluminum.

35. The process of Claim 33, wherein the doping metal is effective to convert the at least a portion of the amorphous region from one of an n-type, intrinsic, or p-type material to another upon crystallization.

36. The process of Claim 35, wherein the doping metal is aluminum.

37. The process of Claim 30, wherein said annealing is conducted for an annealing time in the range of about 1 second to about 24 hours.

38. The process of Claim 37, wherein said annealing is conducted for an annealing time in the range of about 30 seconds to about 1 hour.

39. The process of Claim 38, wherein said annealing is conducted for an annealing time in the range of about 1 minute to about 30 minutes.

40. A process for making a semiconductor junction, comprising:

(a) providing a structure including a semiconductor surface, a semiconductor layer having an amorphous region on the semiconductor surface, and a metal outer layer on the amorphous region;

(b) annealing the structure provided in step (a) at a temperature in the range of about 170°C to about 600°C so as to convert at least a portion of the amorphous region into a crystalline semiconductor having a junction with the semiconductor surface, wherein the metal of a portion of the metal layer promotes the conversion of the at least a portion of the amorphous region into the crystalline semiconductor.

41. The process of Claim 40, wherein said temperature in step (b) is less than about 450°C.

42. The process of Claim 41, wherein said temperature in step (b) is in a range of about 200°C to about 300°C.

43. The process of Claim 40, wherein the metal includes a doping metal which serves to promote the conversion of the at least a portion of the amorphous region into the crystalline semiconductor silicon and to dope the crystalline semiconductor.

44. The process of Claim 43, wherein the doping metal is aluminum.

45. The process of Claim 43, wherein the doping metal is effective to convert the at least a portion of the amorphous region from one of an n-type, intrinsic, or p-type material to another upon crystallization.

46. The process of Claim 45, wherein the doping metal is aluminum.

47. The process of Claim 40, wherein said annealing is conducted for an annealing time in the range of about 1 second to about 24 hours.

48. The process of Claim 47, wherein said annealing is conducted for an annealing time in the range of about 30 seconds to about 1 hour.

49. The process of Claim 48, wherein said annealing is conducted for an annealing time in the range of about 1 minute to about 30 minutes.

50. A process for making a semiconductor junction, comprising:

(a) providing a structure including a semiconductor layer having an amorphous semiconductor region disposed thereon, and metal on the amorphous region with no additional layer being formed over the metal;

(b) annealing the structure provided in step (a) at a temperature in the range of about 170°C to about 600°C so as to convert at least a portion of the amorphous region into a crystalline semiconductor having a junction with the semiconductor layer, wherein the metal includes a portion

that promotes the conversion of the at least a portion of the amorphous region into the crystalline semiconductor.

51. The process of Claim 50, wherein said temperature in step (b) is less than about 450°C.

52. The process of Claim 51, wherein said temperature in step (b) is in a range of about 200°C to about 300°C.

53. The process of Claim 52, wherein the metal includes a doping metal which serves to promote the conversion of the at least a portion of the amorphous region into the crystalline semiconductor and to dope the crystalline semiconductor.

54. The process of Claim 53, wherein the doping metal is aluminum.

55. The process of Claim 53, wherein the doping metal is effective to convert the at least a portion of the amorphous region from one of an n-type, intrinsic, or p-type material to another upon crystallization.

56. The process of Claim 55, wherein the doping metal is aluminum.

57. The process of Claim 50, wherein said annealing is conducted for an annealing time in the range of about 1 second to about 24 hours.

58. The process of Claim 57, wherein said annealing is conducted for an annealing time in the range of about 30 seconds to about 1 hour.

59. The process of Claim 58, wherein said annealing is conducted for an annealing time in the range of about 1 minute to about 30 minutes.

60. A structure for use in manufacturing a semiconductor device consisting of :

(a) a lower single crystalline silicon substrate;

(b) an intermediate amorphous silicon semiconductor layer in contact with said single crystalline silicon substrate; and

(c) an uppermost metal layer in contact with said amorphous silicon semiconductor layer.

61. A structure for use in manufacturing a semiconductor device consisting of comprising:

(a) a lower single crystalline silicon substrate;

(b) an intermediate polycrystalline silicon semiconductor layer in contact with said single crystalline silicon substrate;

(c) an uppermost metal layer in contact with said polycrystalline silicon semiconductor layer.

62. A semiconductor device consisting of :

(a) a lower single crystalline silicon substrate of a first conductivity type;

(b) an intermediate polycrystalline silicon layer in contact with said single crystalline silicon substrate, said polycrystalline silicon layer having a second conductivity type opposite to that of said single crystalline silicon substrate; and

(c) an uppermost metal layer in contact with said intermediate polycrystalline silicon layer.